

Description

The μPD71088 is a CMOS system bus controller for a μPD70108 (V20®) or μPD70116 (V30®) microprocessor system. It controls the memory or I/O system bus.

Features

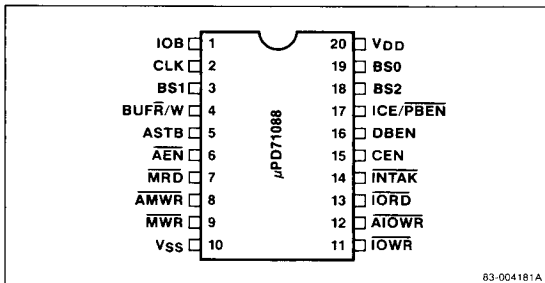
- CMOS technology
- Bus controller for microcomputer system expansion
- Command outputs for system bus control
- Control outputs for I/O peripheral bus control
- High drive capability for command and control outputs ($I_{OL} = 12 \text{ mA}$)
- Three-state outputs for command outputs
- Advanced I/O and memory write command outputs
- μPD70108, μPD70116 compatible
- +5-volt $\pm 10\%$ single power supply
- 20-pin plastic DIP (300 mil) or SOP package
- Industrial temperature range: -40 to $+85^\circ\text{C}$

Ordering Information

| Part Number | Clock (MHz) | Package Type |
|-------------|-------------|--------------------|
| μPD71088C-8 | 8 | 20-pin plastic DIP |
| C-10 | 10 | |
| G-8 | 8 | 20-pin plastic SOP |

Pin Configurations

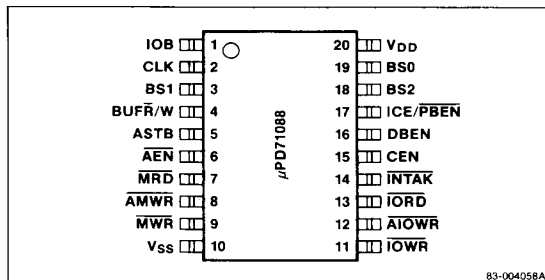
20-Pin Plastic DIP



83-004181A

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20-Pin Plastic SOP



83-004058A

Pin Identification

| Symbol | Function |
|----------|--|
| IOB | Input/output bus mode input |
| CLK | Clock input |
| BS1 | Bus status input 1 |
| BUF̄R/W | Buffer read/write output |
| ASTB | Address strobe output |
| AEN | Address enable input |
| MRD | Memory read output |
| AMWR | Advanced memory write output |
| MWR | Memory write command output |
| Vss | Ground |
| IOWR | I/O write command output |
| AIOWR | Advanced I/O write command output |
| IORD | I/O read command output |
| INTAK | Interrupt acknowledge output |
| CEN | Command enable input |
| DBEN | Data buffer enable output |
| ICE/PBEN | Interrupt cascade enable/Peripheral data bus enable output |
| BS2 | Bus status input 2 |
| BS0 | Bus status input 0 |
| VDD | Power supply |

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PIN FUNCTIONS**BS0-BS2 (Bus Status Inputs 0, 1, 2)**

The BS0-BS2 inputs are connected to the encoded CPU status outputs. The μPD71088 decodes these status outputs into command and control outputs for timing control. See table 1 for an explanation of these inputs.

CLK (Clock)

The CLK input is connected to the same clock output that drives the CPU clock, usually the CLK output of a μPD71084 or a μPD71011. It is the internal system clock of the μPD71088.

 $\overline{\text{AEN}}$ (Address Enable)

The $\overline{\text{AEN}}$ input controls the command output buffers. When IOB is low, a low-level $\overline{\text{AEN}}$ causes the command buffers to output command output signals. A high-level $\overline{\text{AEN}}$ makes all command lines go to high impedance. When IOB is high, the μPD71088 is in I/O bus mode, and the command lines are not affected by $\overline{\text{AEN}}$.

CEN (Command Enable)

The CEN input controls DBEN, $\overline{\text{PBEN}}$ and all command outputs. When CEN is high, all these outputs are active. When CEN is low, they are inactive.

IOB (I/O Bus Mode)

When the IOB input is high, the bus control mode is I/O bus mode. When IOB is low, the bus control mode is system bus mode.

 $\overline{\text{MRD}}$ (Memory Read Command)

The $\overline{\text{MRD}}$ output is the signal to read data from a memory device. $\overline{\text{MRD}}$ is three-state, active low.

 $\overline{\text{MWR}}$ (Memory Write Command)

The $\overline{\text{MWR}}$ output is the signal to write data to a memory device. $\overline{\text{MWR}}$ is three-state, active low.

 $\overline{\text{AMWR}}$ (Advanced Memory Write Command)

This command output is the same as $\overline{\text{MWR}}$, except that it is generated one state (clock cycle) earlier than $\overline{\text{MWR}}$.

 $\overline{\text{IRD}}$ (I/O Read Command)

The $\overline{\text{IRD}}$ output is the signal to read data from an I/O device. $\overline{\text{IRD}}$ is three-state, active low.

 $\overline{\text{IOWR}}$ (I/O Write Command)

The $\overline{\text{IOWR}}$ output is the signal to write data to an I/O device. $\overline{\text{IOWR}}$ is three-state, active low.

 $\overline{\text{AIOWR}}$ (Advanced I/O Write Command)

This command output is the same as $\overline{\text{IOWR}}$, except that it is generated one state (clock cycle) earlier than $\overline{\text{IOWR}}$.

 $\overline{\text{INTAK}}$ (Interrupt Acknowledge)

The $\overline{\text{INTAK}}$ output acknowledges interrupt requests. Requesting devices output an interrupt vector address in response to $\overline{\text{INTAK}}$. $\overline{\text{INTAK}}$ is three-state, active low.

ASTB (Address Strobe)

The ASTB output control signal latches the address outputs from the CPU into an external address latch, such as a μPD71082 or μPD71083. Address data should be strobed with the trailing edge (high to low) of ASTB.

DBEN (Data Buffer Enable)

The DBEN output activates a data bus buffer/driver such as a μPD71086 or μPD71087 to input or output data between the CPU local bus and the memory or I/O system bus.

 $\overline{\text{BUF\overline{R}/W}}$ (Buffer Read/Write)

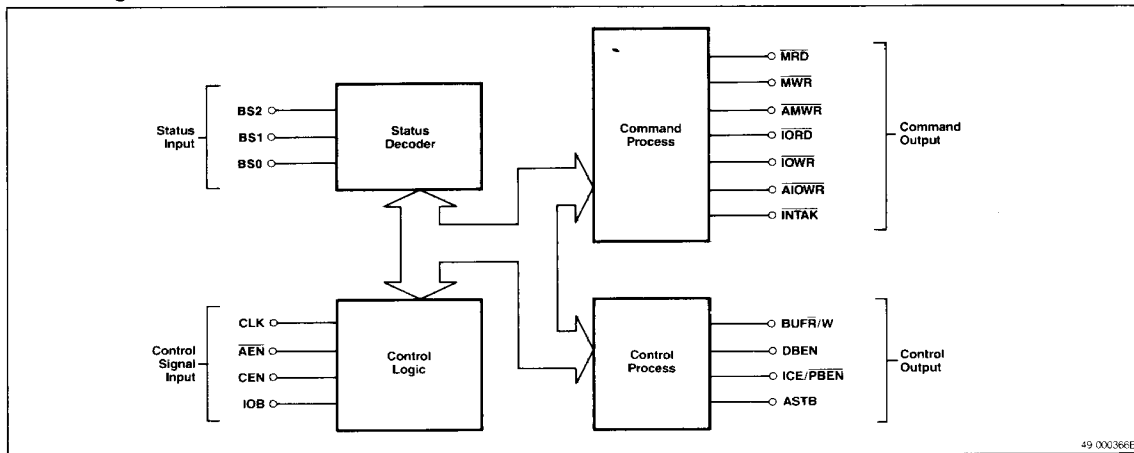
The $\overline{\text{BUF\overline{R}/W}}$ output controls the direction in which data moves through a transceiver between the CPU and the memory or I/O peripherals. When $\overline{\text{BUF\overline{R}/W}}$ is high, data is transferred from the CPU local bus to the memory or I/O system bus. When $\overline{\text{BUF\overline{R}/W}}$ is low, data is transferred from the memory or I/O system bus to the CPU local bus.

 $\overline{\text{ICE/PBEN}}$ (Interrupt Cascade Enable/Peripheral Data Bus Enable)

The meaning of this output signal depends on IOB. If IOB is low (system bus mode), it is the ICE output. ICE controls the cascade address transfer from a master priority interrupt controller to slave priority interrupt controllers. The slave reads the address from the master when ICE goes high.

When IOB is high, it becomes $\overline{\text{PBEN}}$. $\overline{\text{PBEN}}$ controls the I/O bus the same way that DBEN controls the system bus. In this case, however, the output is active low.

Block Diagram



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Absolute Maximum Ratings

$T_A = 25^\circ\text{C}; V_{SS} = 0\text{ V}$

| | |
|----------------------------------|---------------------------------|
| Power supply voltage, V_{DD} | -0.5 to +7.0 V |
| Input voltage, V_I | -1.0 to $V_{DD} + 1.0\text{ V}$ |
| Output voltage, V_O | -0.5 to $V_{DD} + 0.5\text{ V}$ |
| Operating temperature, T_{OPR} | -40 to +85 °C |
| Storage temperature, T_{STG} | -65 to +150 °C |
| Power dissipation, P_D (DIP) | 500 mW |
| Power dissipation, P_D (SO) | 200 mW |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Capacitance

$T_A = 25^\circ\text{C}; V_{DD} = +5\text{ V}$

| Parameter | Symbol | Min | Max | Units | Conditions |
|-------------------|----------|-----|-----|-------|--------------------|
| Input capacitance | C_{IN} | | 12 | pF | $f = 1\text{ MHz}$ |

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DC Characteristics

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}; V_{DD} = 5\text{ V} \pm 10\%$

| Parameter | Symbol | Min | Max | Unit | Conditions |
|-----------------------------------|-------------|----------------|------|------|--|
| Input voltage, high | V_{IH} | 2.2 | | V | |
| Input voltage, low | V_{IL} | | 0.8 | V | |
| Output voltage, high | V_{OH} | $V_{DD} - 0.8$ | | V | Controls: $I_{OH} = -8\text{ mA @ } 10\text{ MHz}, -4\text{ mA @ } 8\text{ MHz}$ |
| Output voltage, low | V_{OL} | | 0.45 | V | Commands: $I_{OL} = 24\text{ mA @ } 10\text{ MHz}, 12\text{ mA @ } 8\text{ MHz}$ Controls: $I_{OL} = 8\text{ mA @ } 10\text{ MHz}, 4\text{ mA @ } 8\text{ MHz}$ |
| Input current leakage | I_{IL} | -1.0 | 1.0 | μA | $V_I = V_{DD}, V_{SS}$ |
| Leakage current at high impedance | I_{OFF} | -10 | 10 | μA | |
| Power supply current (static) | I_{DD} | | 80 | μA | $V_I = V_{DD}, V_{SS}$ |
| Power supply current (dynamic) | I_{DDdyn} | | 20 | mA | $f_{in} = 10\text{ MHz}$ |

5K - 3

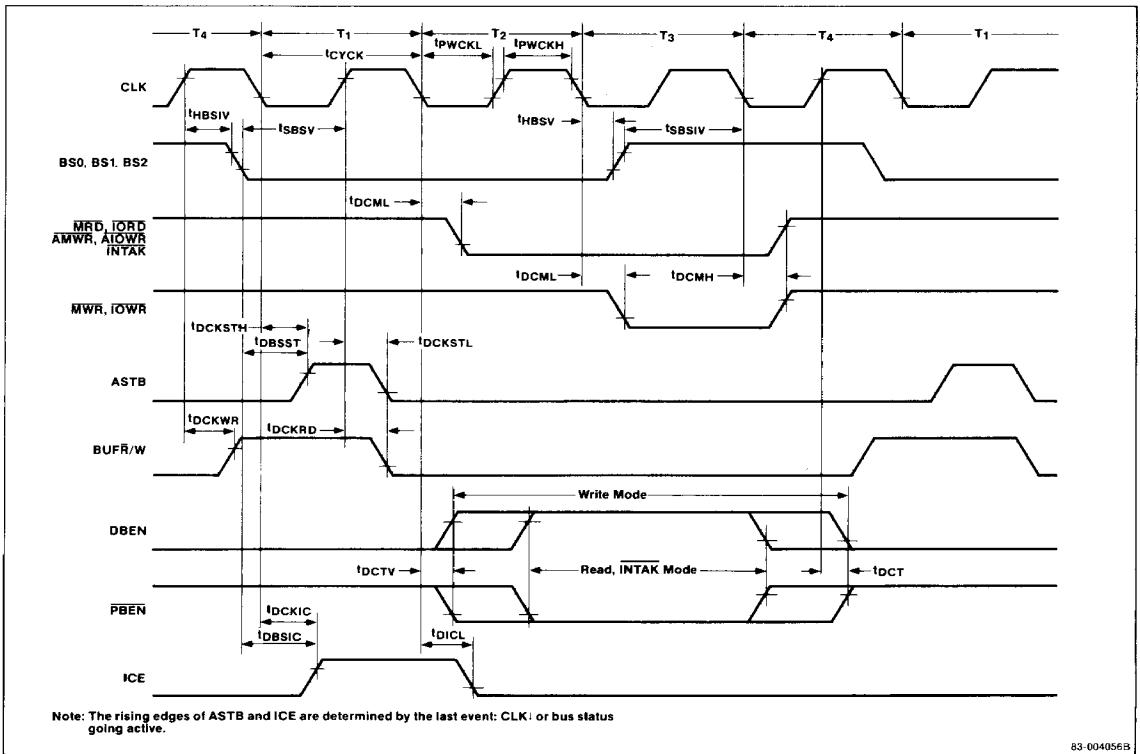
AC Characteristics

T_A = -40 to +85°C; V_{DD} = 5 V ± 10%

| Parameter | Symbol | μPD71088 | | μPD71088C-10 | | Units | Conditions |
|--|---------------------|----------|-------------------|--------------|-------------------|-------|--|
| | | Min | Max | Min | Max | | |
| CLK cycle period | t _{CYCK} | 125 | | 100 | | ns | |
| CLK pulse width, high | t _{PWCKH} | 40 | | 41 | | ns | |
| CLK pulse width, low | t _{PWCKL} | 60 | | 49 | | ns | |
| Setup time for bus status active to CLK ↑ | t _{SBSV} | 40 | | 35 | | ns | |
| Hold time for bus status inactive from CLK ↓ | t _{HBSV} | 10 | | 10 | | ns | |
| Setup time for bus status inactive to CLK ↓ | t _{SBSIV} | 35 | | 35 | | ns | |
| Hold time for bus status inactive from CLK ↑ | t _{HBSIV} | 10 | | 10 | | ns | |
| Command active delay from CLK ↓ | t _{DCML} | 10 | 40 | 10 | 35 | ns | |
| Command inactive delay from CLK ↓ | t _{DCMH} | 10 | 40 | 10 | 35 | ns | |
| Command output on delay from \overline{AEN} ↓ | t _{DAECM} | | 40 | | 40 | ns | |
| Command active output delay from \overline{AEN} ↓ | t _{DAECML} | 100 | 295 | 115 | 200 | ns | |
| Command disable delay from \overline{AEN} ↑ | t _{FAECM} | | 50 | | 20 | ns | |
| Command active delay from CEN ↑ | t _{DCECM} | | t _{DCML} | | t _{DCML} | ns | I _{OL} = 4 mA I _{OH} = -4 mA C _L = 100 pF |
| ASTB active delay from CLK ↓ | t _{DCKSTH} | | 30 | | 20 | ns | |
| ASTB active delay from BS2, 1, 0 | t _{DBSST} | | 25 | | 20 | ns | |
| ASTB inactive delay from CLK ↑ | t _{DCKSTL} | 7 | 25 | 7 | 25 | ns | |
| DBEN, \overline{PBEN} active delay from CLK ↓ | t _{DCTV} | 10 | 50 | 10 | 35 | ns | |
| DBEN, \overline{PBEN} inactive delay from CLK ↑ | t _{DCT} | 10 | 50 | 10 | 35 | ns | |
| DBEN, \overline{PBEN} active delay from \overline{AEN} ↓ | t _{DAECT} | | 30 | | 30 | ns | |
| DBEN, \overline{PBEN} active delay | t _{DCECT} | | 30 | | 30 | ns | |
| BUFR/W ↑ delay from CLK ↑ | t _{DCKWR} | | 40 | | 40 | ns | |
| BUFR/W ↓ delay from CLK ↑ | t _{DCKRD} | | 60 | | 40 | ns | |
| ICE active delay from CLK ↓ | t _{DCKIC} | | 30 | | 30 | ns | |
| ICE active delay from BS2, 1, 0 | t _{DBSIC} | | 25 | | 20 | ns | |
| ICE inactive delay from CLK ↓ | t _{DICL} | 10 | 50 | 10 | 40 | ns | |
| Input rise time | t _{RI} | | 20 | | 20 | ns | 0.8 V to 2.0 V |
| Output rise time | t _{RO} | | 20 | | 20 | ns | |
| Input fall time | t _{FI} | | 12 | | 12 | ns | 2.0 V to 0.8 V |
| Output fall time | t _{FO} | | 12 | | 12 | ns | |

Timing Waveforms

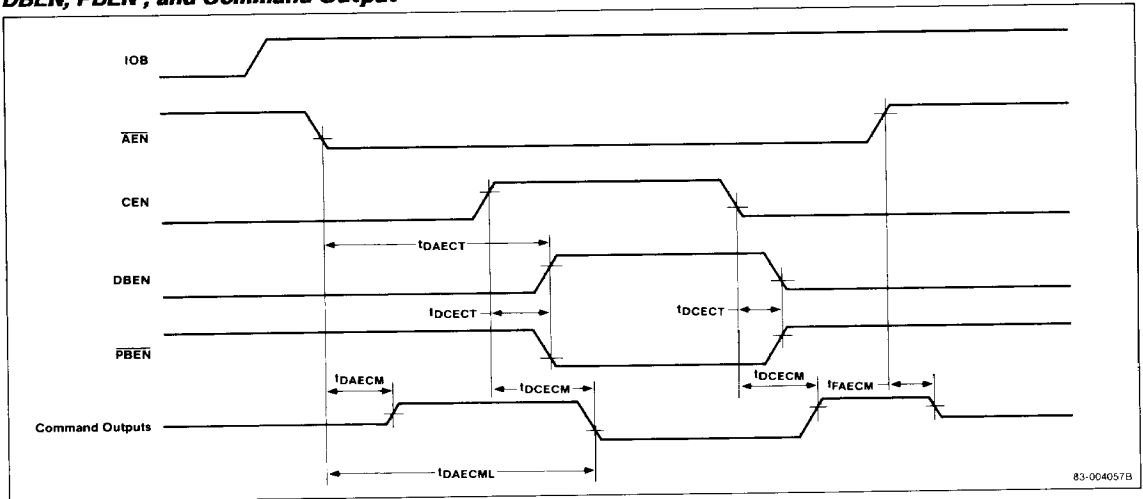
General



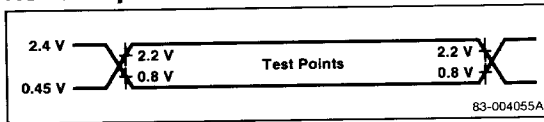
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Timing Waveforms (cont)

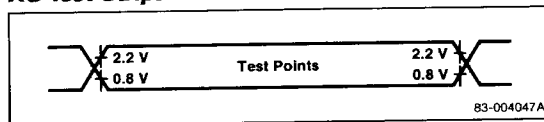
DBEN, $\overline{\text{PBEN}}$, and Command Output



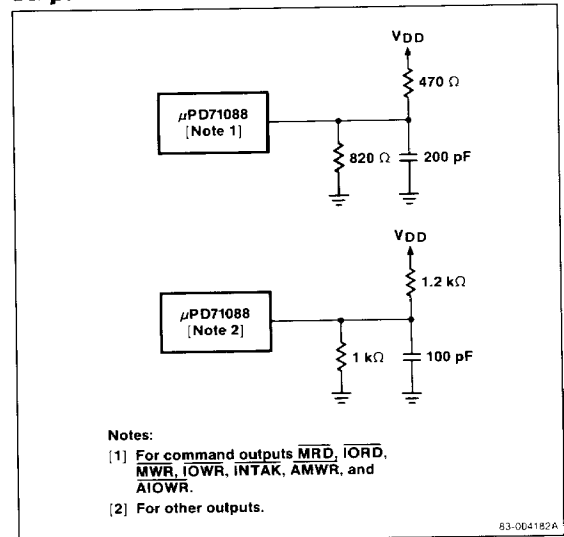
AC Test Input



AC Test Output



Output Test Loads



Notes:

- [1] For command outputs $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, $\overline{\text{INTAK}}$, $\overline{\text{AMWR}}$, and $\overline{\text{AIOWR}}$.
- [2] For other outputs.

FUNCTIONAL DESCRIPTION

Command Logic

The PD71088 decodes the CPU bus status outputs into command outputs. The bus status outputs (BS0-BS2) and their decoded commands are shown in table 1.

Bus Control Mode

The CEN, IOB, and $\overline{\text{AEN}}$ signals control the bus controller mode as shown in table 2.

Table 1. Command Logic

| | | | | μPD71088 |
|------|------|------|------------------------|---|
| BS2 | BS1 | BS0 | CPU Status | Command Output |
| Low | Low | Low | Interrupt acknowledge | $\overline{\text{INTAK}}$ |
| Low | Low | High | I/O read mode | $\overline{\text{IORD}}$ |
| Low | High | Low | I/O write mode | $\overline{\text{IOWR}}, \overline{\text{AIOWR}}$ |
| Low | High | High | Halt mode | None |
| High | Low | Low | Instruction fetch mode | $\overline{\text{MRD}}$ |
| High | Low | High | Memory read mode | $\overline{\text{MRD}}$ |
| High | High | Low | Memory write mode | $\overline{\text{MWR}}, \overline{\text{AMWR}}$ |
| High | High | High | No bus cycle mode | None |

Table 2. Bus Control Mode

| Control Input | | Command Output | | | Control Output | |
|-----------------------------|------------------------|-------------------------|--|--|-------------------------------|--|
| CEN | IOB | $\overline{\text{AEN}}$ | Memory | I/O | ICE/PBEN | ASTB, $\overline{\text{BUFR/W}}$, DBEN |
| | | | $\overline{\text{MRD}}, \overline{\text{MWR}}, \overline{\text{AMWR}}$ | $\overline{\text{IOWR}}, \overline{\text{AIOWR}}, \overline{\text{IORD}}, \overline{\text{INTAK}}$ | | |
| H | H (I/O bus mode) | H | High impedance | Outputs enabled (NC) | $\overline{\text{PBEN}}$ (NC) | Outputs enabled (NC) |
| | | L | Outputs enabled | | | |
| H | L (System bus mode) | H | High impedance | High impedance | ICE (NC) | Outputs enabled (NC) |
| | | L | Output enabled | Outputs enabled | | |
| L (Command disable mode) | x | x | H | H | PBEN = H | Outputs enabled (DBEN = L:ASTB, $\overline{\text{BUFR/W}}$ are NC) |

Note:

x = Don't care, NC = No change, H = High, L = Low

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